WHAT IS CLAIMED IS:

1. A reconfigurable chip comprising:

a despreader function block including complex multiplier units, the despreader function block including multiplexers to allow the selection of different operation configurations for the despreader function block; and

interconnect elements operably connected to the despreader function block the interconnect elements adapted to selectively connect together the despreader function block with other reconfigurable units.

2. The reconfigurable chip of Claim 1 wherein the complex multiplier unit comprises a complex half multiplier unit.

3. The reconfigurable chip of Claim 1 wherein the complex half multiplier unit comprises a 1-bit complex half multiplier unit.

4. The reconfigurable chip of Claim 3 wherein the 1-bit complex half multiplier is implemented using at least one multiplexer and an inverter.

5. The reconfigurable chip of Claim 1 wherein the despreader function box can also implement a correlation function.

6. The reconfigurable chip of Claim 1 wherein the despreader function block includes a number of despreader trees.

7. The reconfigurable chip of Claim 1 wherein the despreader trees include a number of complex half multiplier units connected to adder units.

8. The reconfigurable chip of Claim 1 wherein the despreader function block is controlled by an instruction stored in an associated instruction memory.

9. The reconfigurable chip of Claim 1 wherein the despreader function block includes multiple block input multiplexers and at least one block output multiplexer.

10. A reconfigurable chip including:

a despreader function block including complex multiplier units, the despreader function block including multiplexers to allow the selection of different operation configurations for the despreader function block; and

an instruction memory storing multiple instructions for the despreader function block

11. The reconfigurable chip of Claim 10 wherein the complex multiplier unit comprises a complex half multiplier unit.

12. The reconfigurable chip of Claim 11 wherein the complex half multiplier units include at least one multiplexer and an inverter.

13. The reconfigurable chip of Claim 10 wherein the despreader function block can also implement a correlator function.

14. The reconfigurable chip of Claim 10 wherein the despreader function block can also implement a multiplication function.

15. The reconfigurable chip of Claim 10 wherein the despreader function block includes despreader trees.

16. The reconfigurable chip of Claim 15 wherein the despreader trees include complex half multiplier units and adders.

17. The reconfigurable chip of Claim 10 wherein the despreader function block includes multiple block input multipliers and at least one block output multiplexer.

18. The reconfigurable chip of Claim 10 further comprising interconnect elements operably connected to the despreader function block, the interconnect elements adapted to selectively connect the other despreader function block with other reconfigurable units.

19. A despreader function block on a reconfigurable chip, the despreader function block including:

multiple block input multiplexers;

despreader tree units including complex multiplier units, the despreader tree units operably connected to the multiple block input multiplexers; and

at least one block output multiplexer operably connected to the selectable despreader tree units.

20. The despreader function block of Claim 19 wherein the complex multiplier units comprise complex half multiplier units.

21. The despreader function block of Claim 19 wherein the complex half multiplier units comprise a multiplexer and an inverter.

22. The despreader function block of Claim 19 wherein the despreader tree units further include adder elements.

23. A reconfigurable chip including the despreader function block of Claim 19.

24. The reconfigurable chip of Claim 23 further comprising an interconnect element operably connected to the despreader function block to operably connect together the despreader function block with other reconfigurable units.

25. The reconfigurable chip of Claim 23 further comprising an instruction memory showing multiple instructions for the despreader function block.

26. The despreader function block of Claim 19 wherein the despreader tree units can also implement correlation functions.

27. The despreader function block of Claim 19 wherein the despreader function block can also implement a multiplication function.

28. A reconfigurable chip comprising:

multiple despreader blocks, the despreader blocks adapted to despread input signals using an PN sequence, the selectable blocks also being selectable to a non-despreader function; and

reconfigurable functional units operably connectable to the despreader blocks, the reconfigurable functional units including an arithmetic logic unit.

29. The reconfigurable chip of Claim 28 wherein the despreader function block include complex half multiplier units.

30. The reconfigurable chip of Claim 28 wherein the complex half multiplier units are implemented using multiplexers and an inverter.

31. The reconfigurable chip of Claim 28 wherein the despreader function blocks are implemented using a despreader tree.

32. The reconfigurable chip of Claim 31 wherein the despreader tree is implemented using a number of complex half multiplier units and adders.

33. The reconfigurable chip of Claim 28 wherein the despreader blocks can also implement a correlator function.

34. The reconfigurable chip of Claim 28 wherein the despreader blocks can also implement a multiplication function.

35. The reconfigurable chip of Claim 28 further comprising interconnect elements operably connected to the despreader function block to interconnect between the reconfigurable functional units and the despreader blocks.

36. The reconfigurable chip of Claim 28 wherein input multiplexers for the despreader blocks can be selected to connect to operative nearby reconfigurable functional units.

37. The reconfigurable chip of Claim 28 wherein the despreader function block includes multiplexers and at least one block output multiplexer.

38. The reconfigurable chip of Claim 28 further comprising an instruction memory storing multiple instructions for the despreader function block.